GaAs, pHEMT, MMIC, 1 W Power Amplifier, 0.1 GHz to 6 GHz

Enhanced Product

HMC637ASCPZ-EP

FEATURES

P1dB output power: 29 dBm typical
Gain: 13 dB typical
OIP3: 44 dBm typical
50 Ω matched input/output
32-lead, 5 mm × 5 mm LFCSP package: 25 mm²

ENHANCED PRODUCT FEATURES

Supports defense and aerospace applications (AQEC standard)
Extended industrial temperature range (−55°C to +105°C)
Controlled manufacturing baseline
1 assembly/test site
1 fabrication site
Product change notification
Qualification data available on request

APPLICATIONS

Telecom infrastructure
Microwave radio
Very small aperture terminal (VSAT)
Military and space
Test instrumentation
Fiber optics

FUNCTIONAL BLOCK DIAGRAM

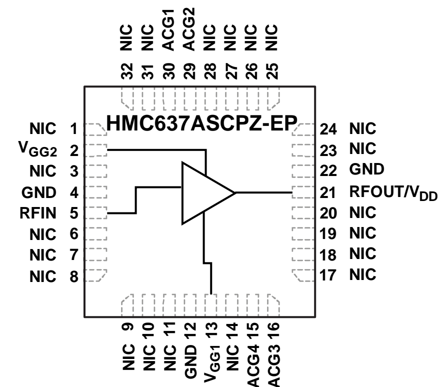

Figure 1.

GENERAL DESCRIPTION

The HMC637ASCPZ-EP is a gallium arsenide (GaAs), monolithic microwave integrated circuit (MMIC), pseudomorphic high electron mobility transistor (pHEMT), distributed power amplifier that operates between 0.1 GHz and 6 GHz. The amplifier provides 13 dB of gain, 44 dBm output third-order intercept (OIP3), and 29 dBm of output power at 1 dB gain compression (P1dB) while requiring 400 mA from a 12.0 V supply. Gain flatness is ±0.75 dB from 0.1 GHz to 6 GHz, making the HMC637ASCPZ-EP ideal for electronic warfare (EW), electronic counter-measure (ECM), radar and test equipment applications. The HMC637ASCPZ-EP amplifier radio frequency (RF) inputs/outputs (I/Os) are internally matched to 50 Ω, and the 5 mm × 5 mm lead frame chip scale package (LFCSP) is compatible with high volume surface-mount technology (SMT) assembly equipment.

Additional application and technical information can be found in the HMC637ALP5E data sheet.

Rev. 0 Document Feedback

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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support
www.analog.com

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TABLE OF CONTENTS

Features ... 1
Enhanced Product Features ... 1
Applications ... 1
Functional Block Diagram ... 1
General Description ... 1
Revision History ... 2
Specifications ... 3
  Electrical Specifications ... 3
Absolute Maximum Ratings ... 4
  Thermal Resistance ... 4
  Power Derating Curves ... 4
  ESD Caution ... 4
Pin Configuration and Function Descriptions ... 5
  Interface Schematics ... 6
Typical Performance Characteristics ... 7
Outline Dimensions ... 9
  Ordering Guide ... 9

REVISION HISTORY

6/2019—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

T_A = 25°C, V_{DD} = 12 V, V_{GG2} = 5 V, supply current (I_{DD}) = 400 mA (adjust V_{GG1} between −2 V to 0 V to achieve I_{DD} = 400 mA typical), 50 Ω system, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE			0.1		6	GHz
GAIN			12	13		dB
Gain Flatness				±0.75		dB
Gain Variation Over Temperature				0.015		dB/°C
RETURN LOSS						
Input				12		dB
Output				15		dB
OUTPUT						
Output Power for 1 dB Compression	P1dB		27	29		dBm
Saturated Output Power	P_{SAT}			31		dBm
Output Third-Order Intercept	OIP3	Output power (P_{OUT}) per tone = 10 dBm, 1 MHz spacing		44		dBm
NOISE FIGURE				12		dB
		2.0 GHz to 6.0 GHz		5		dB
SUPPLY CURRENT	I_{DD}		320	400	480	mA
Drain Bias Voltage[1]	V_{DD}	I_{DD} = 400 mA		11.5		V
				12.0		V
				12.5		V

[1] V_{GG1} is initially set for nominal bias conditions of V_{DD} = 12 V and V_{GG2} = 5 V to achieve a I_{DD} = 400 mA typical, and then, adjust V_{DD} ± 0.5 V from 12 V to measure the I_{DD} variation.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
V_{DD}	14 V_{DC}
V_{GG1}	−3 V_{DC} to 0 V_{DC}
V_{GG2}	4 V_{DC} to 7 V_{DC}
RF Input Power (RFIN), V_{DD} = 12 V_{DC}	25 dBm
Channel Temperature	175°C
Continuous Power Dissipation, P_{DISS}	See Figure 2
Case Temperature (T_{CASE}) = 85°C	8.6 W
T_{CASE} = 105°C	6.7 W
Maximum Peak Reflow Temperature	260°C (MSL3[1] Rating)
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +105°C
Electrostatic Discharge (ESD) Sensitivity	
Human Body Model (HBM)	Class 1B

[1] MSL3 stands for Moisture Sensitivity Level 3.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the junction to case thermal resistance.

Table 3. Thermal Resistance

Package Type	θ_{JC}[1]	Unit
CP-32-29	10.5	°C/W

[1] Thermal impedance simulated values are based on a JEDEC 1S0P thermal test board. See JEDEC JESD-51.

POWER DERATING CURVES

Figure 2 shows the maximum power dissipation vs. case temperature.

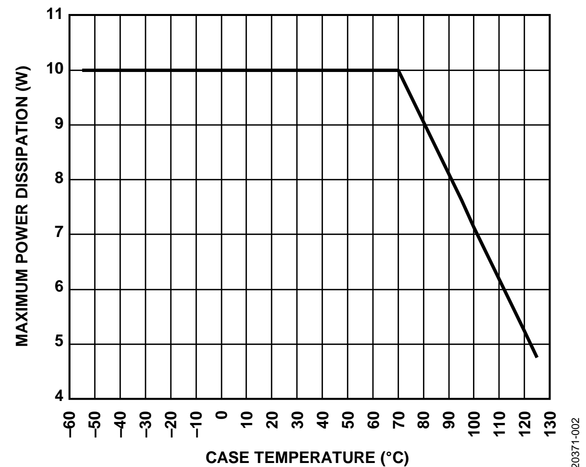
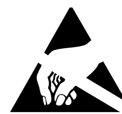


Figure 2. Maximum Power Dissipation vs. Case Temperature

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

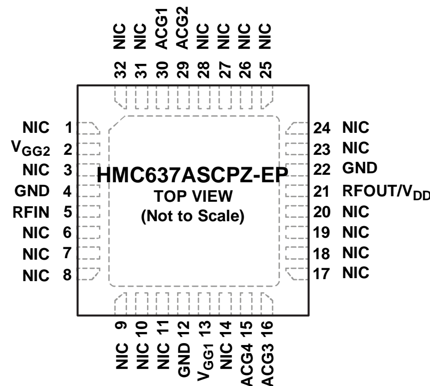


Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description[1]
1, 3, 6 to 11, 14, 17 to 20, 23 to 28, 31, 32	NIC	No Internal Connection. These pins may be connected to RF ground. Performance is not affected.
2	V_{GG2}	Gate Bias Voltage Control 2 for Amplifier. Apply 5 V to V_{GG2} for nominal operation. Attach a bypass capacitor per the application circuit shown the Application Information section of the HMC637ALP5E data sheet.
4, 12, 22	GND	Ground. Connect Pin 4, Pin 12, and Pin 22 to RF and dc ground.
5	RFIN	RF Input. This pad is dc-coupled and matched to 50 Ω.
13	V_{GG1}	Gate Bias Voltage Control 1 for Amplifier. Attach a bypass capacitor per the application circuit shown in the Application Information section of the HMC637ALP5E data sheet. Follow the power-up and power-down sequences outlined in the Application Information section of the HMC637ALP5E data sheet.
15	ACG4	Low Frequency Termination 4. Attach a bypass capacitor per the application circuit shown in the Application Information section of the HMC637ALP5E data sheet.
16	ACG3	Low Frequency Termination 3. Attach a bypass capacitor per the application circuit shown in the Application Information section of the HMC637ALP5E data sheet.
21	RFOUT/V_{DD}	RF Output/Drain Bias Voltage for Amplifier. Connect the dc bias (V_{DD}) network to provide I_{DD}. See the application circuit shown in the Application Information section of the HMC637ALP5E data sheet.
29	ACG2	Low Frequency Termination 2. Attach a bypass capacitor per the application circuit shown in the Application Information section of the HMC637ALP5E data sheet.
30	ACG1	Low Frequency Termination 1. Attach a bypass capacitor per the application circuit shown in the Application Information section of the HMC637ALP5E data sheet.
	EPAD	Exposed Pad. The exposed pad must be connected to RF and dc ground.

[1] See the Interface Schematics section for pin interfaces.

INTERFACE SCHEMATICS

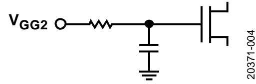


Figure 4. V_{GG2} Interface Schematic

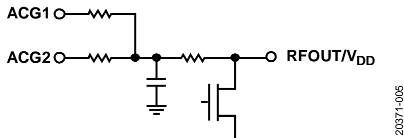


Figure 5. ACG1, ACG2, and RFOUT/V_{DD} Interface Schematic

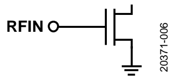


Figure 6. RFIN Interface Schematic

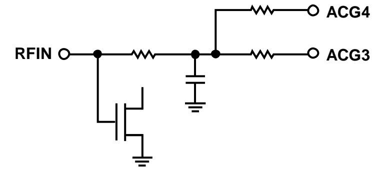


Figure 7. RFIN, ACG4, and ACG3 Interface Schematic

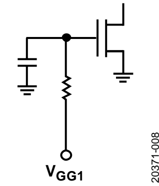


Figure 8. V_{GG1} Interface Schematic

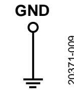


Figure 9. GND Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

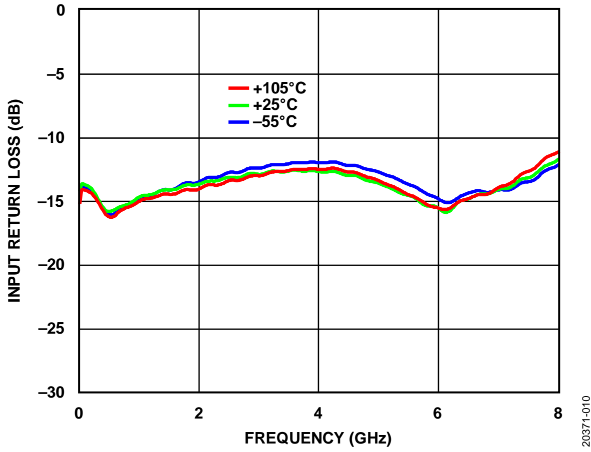


Figure 10. Input Return Loss vs. Frequency at Various Temperatures

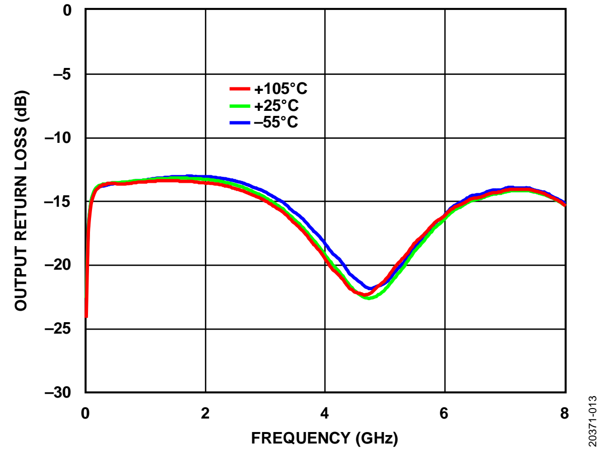


Figure 13. Output Return Loss vs. Frequency at Various Temperatures

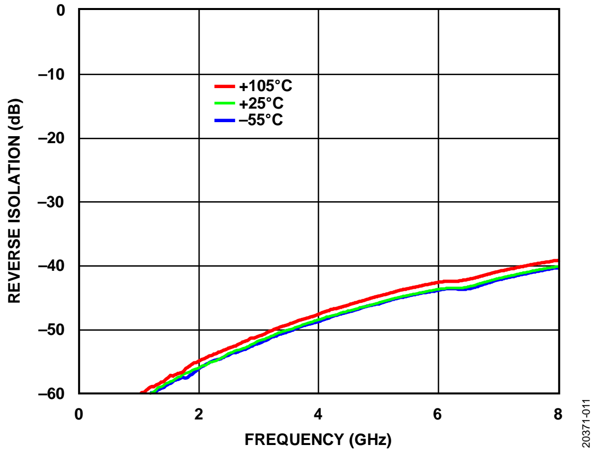


Figure 11. Reverse Isolation vs. Frequency at Various Temperatures

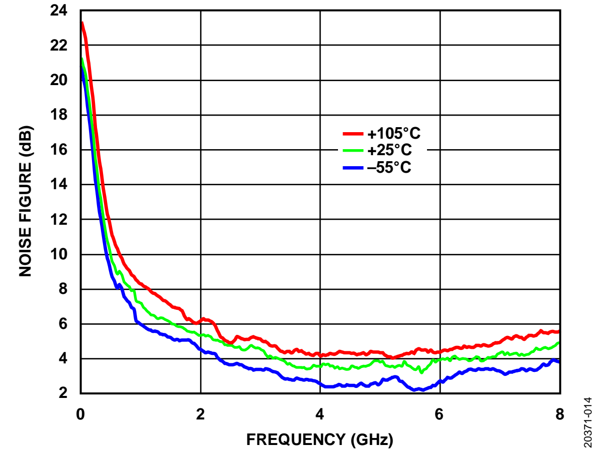


Figure 14. Noise Figure vs. Frequency at Various Temperatures

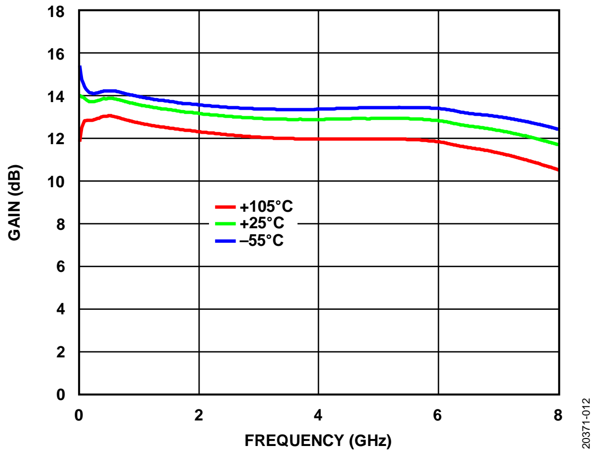


Figure 12. Gain vs. Frequency at Various Temperatures

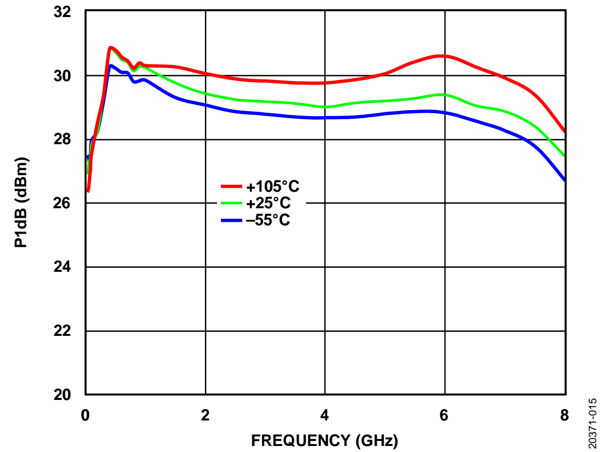


Figure 15. P1dB vs. Frequency at Various Temperatures

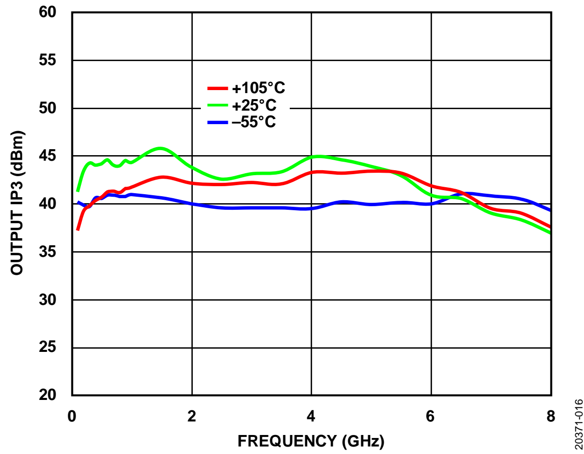


Figure 16. Output IP3 vs. Frequency at Various Temperatures

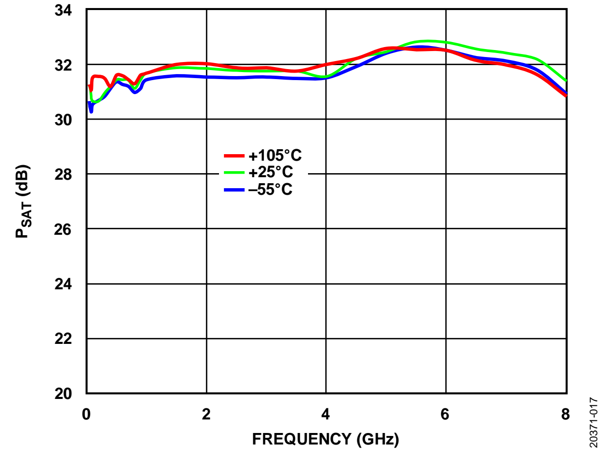


Figure 17. P_{SAT} vs. Frequency at Various Temperatures

OUTLINE DIMENSIONS

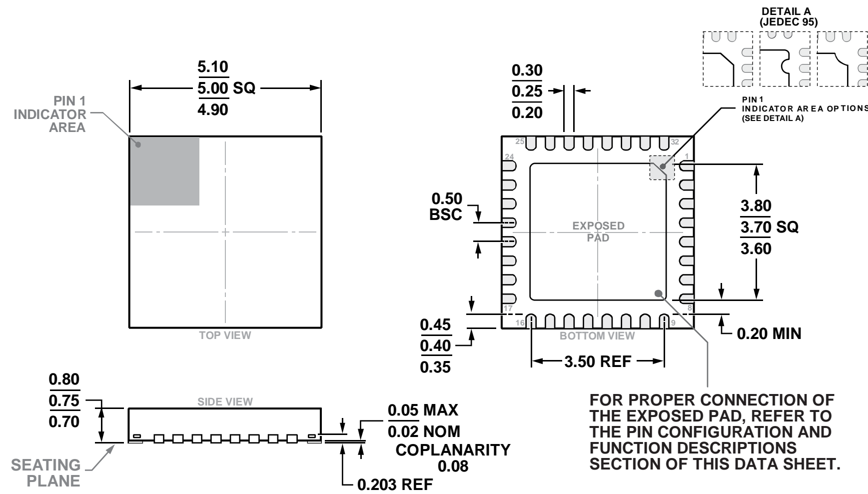


Figure 18. 32-Lead Lead Frame Chip Scale Package [LFCSP]
5 mm × 5 mm and 0.75 mm Package Height
(CP-32-29)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	MSL Rating[2]	Package Description	Package Option
HMC637ASCPZ-EP-PT	−55°C to +105°C	MSL3	32-Lead Lead Frame Chip Scale Package [LFCSP]	CP-32-29
HMC637ASCPZ-EP-R7	−55°C to +105°C	MSL3	32-Lead Lead Frame Chip Scale Package [LFCSP]	CP-32-29

[1] The HMC637ASCPZ-EP is RoHS compliant.
[2] See the Absolute Maximum Ratings section for additional information.

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